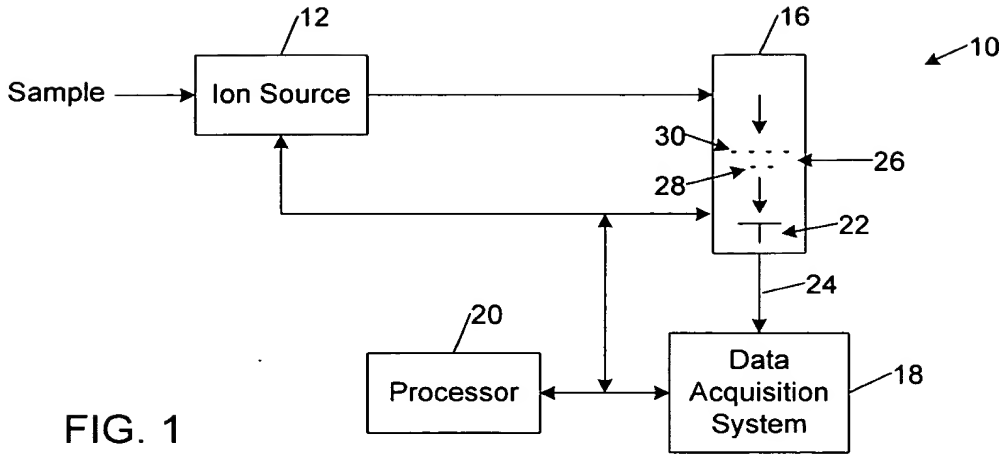

FIG. 1

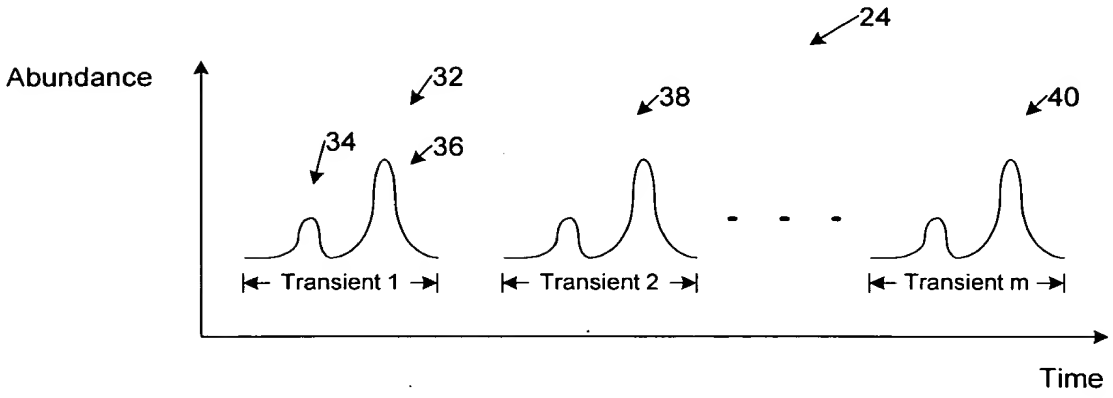

FIG. 2A

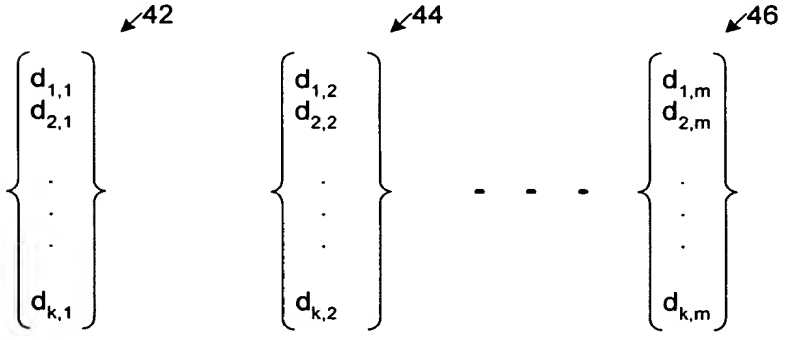

FIG. 2B

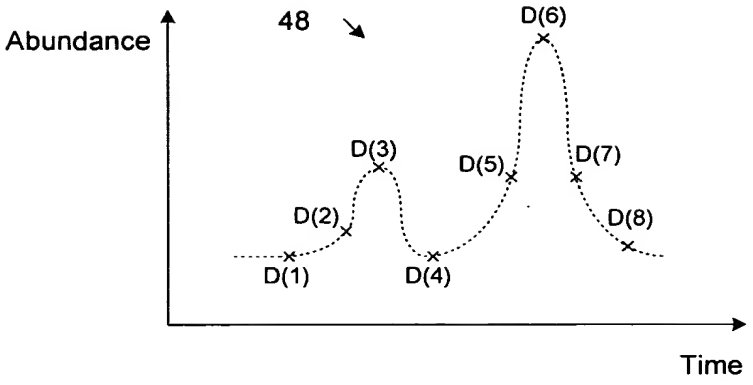

FIG. 2C

$$\left\{\begin{array}{l} D(1) = \sum_i^m d_{1,i} \\ D(2) = \sum_i^m d_{2,i} \\ \vdots \\ D(k) = \sum_i^m d_{k,i} \end{array}\right\}$$

50

FIG. 2D

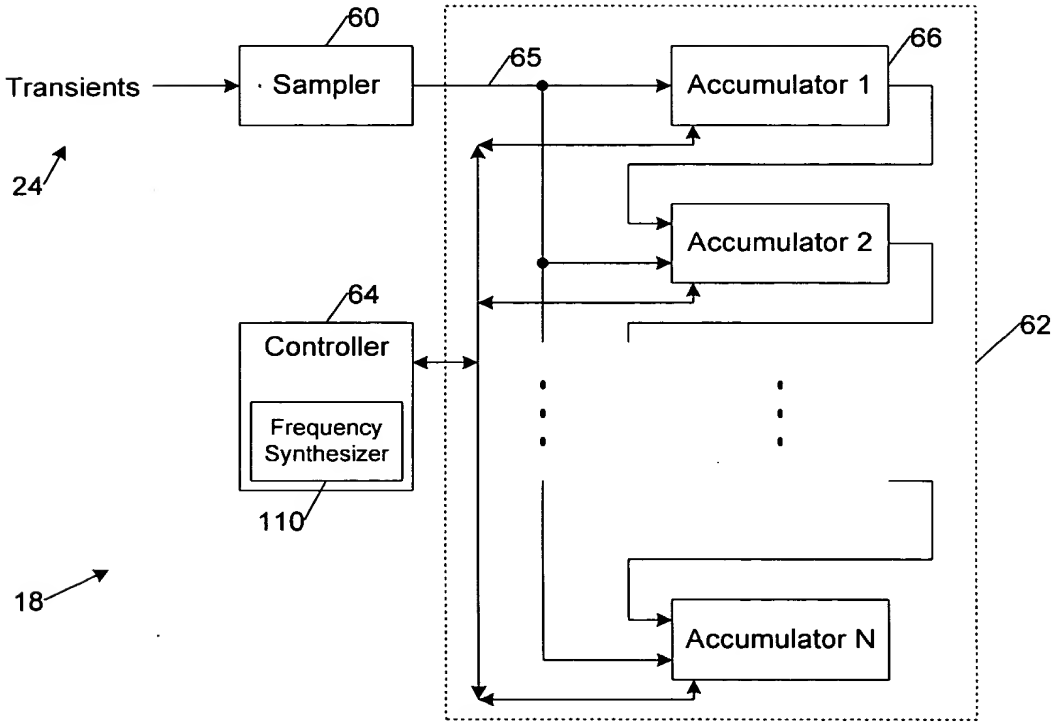

FIG. 3

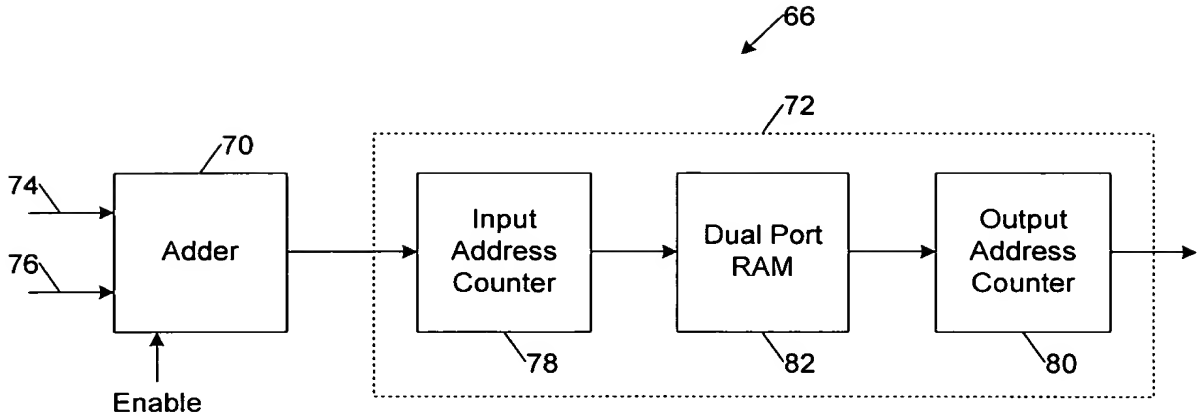
66
72
70
74
76
Adder
Input Address Counter
Dual Port RAM
Output Address Counter
78
82
80
Enable

FIG. 4

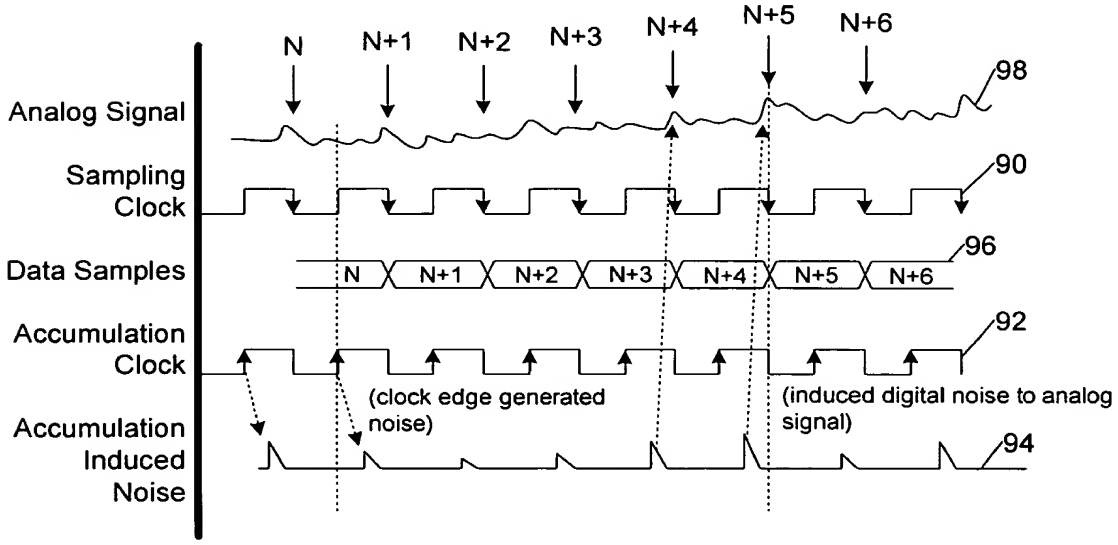
N
N+1
N+2
N+3
N+4
N+5
N+6
98
Analog Signal
Sampling Clock
90
Data Samples
96
Accumulation Clock
92
(clock edge generated noise)
(induced digital noise to analog signal)
Accumulation Induced Noise
94

FIG. 5

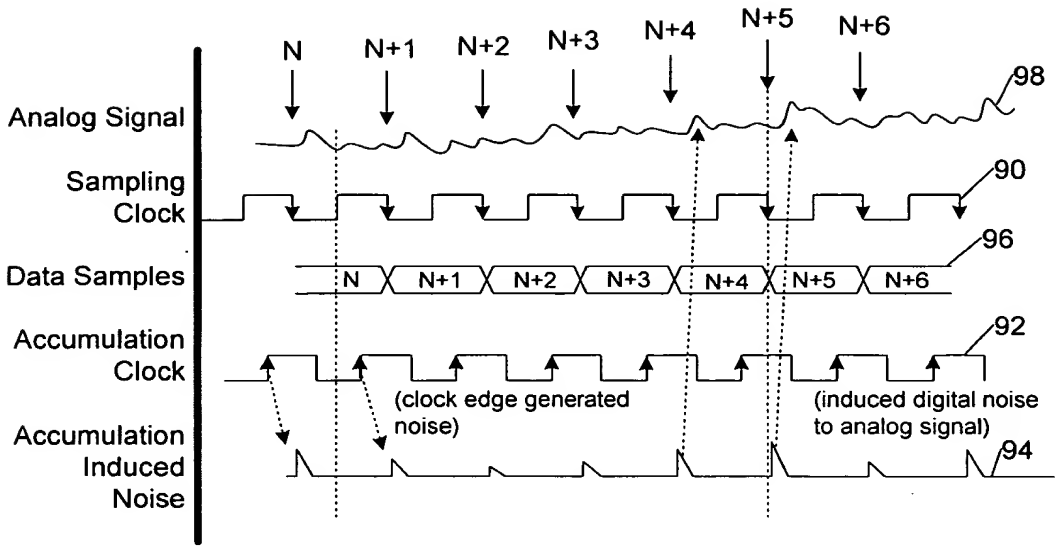
N
N+1
N+2
N+3
N+4
N+5
N+6
Analog Signal
98
Sampling Clock
90
Data Samples
96
Accumulation Clock
92
(clock edge generated noise)
(induced digital noise to analog signal)
Accumulation Induced Noise
94

FIG. 6

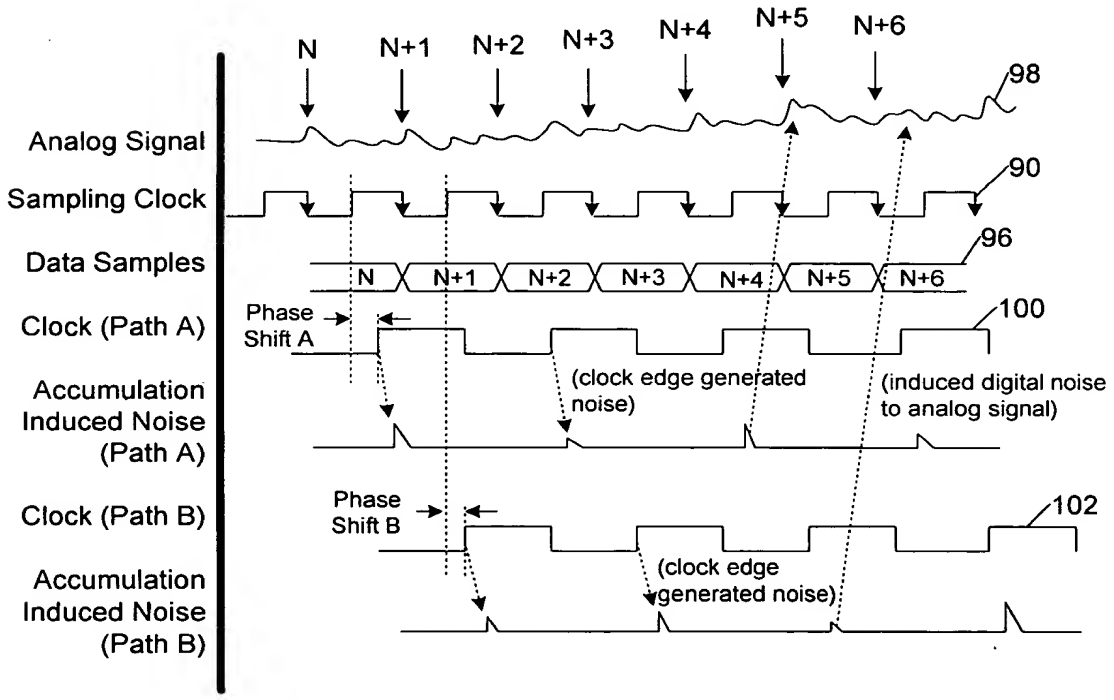
N
N+1
N+2
N+3
N+4
N+5
N+6
Analog Signal
98
Sampling Clock
90
Data Samples
96
Clock (Path A)
Phase Shift A
100
(clock edge generated noise)
(induced digital noise to analog signal)
Accumulation Induced Noise (Path A)
Clock (Path B)
Phase Shift B
102
(clock edge generated noise)
Accumulation Induced Noise (Path B)

FIG. 7